The Office has rejected Claims 32-48 under 35 U.S.C. Section 112, first paragraph, asserting that the present specification fails to provide adequate support for the specific detailed operation/function of the control system, as claimed in claims 32 and 41, which controls the signal from signal stream to substantially charged one of the signal buses which is not being currently read at the output (claim 32) and allowing the signal from the signal streams to substantially charge one of the signal buses that is not being read at the output while other one of the signal is being read (claim 41). The Office has asserted that the exact manner of how the above mentioned operation being achieved has not been clearly defined and or discussed in the present specification.

Applicants respectfully traverse the Office's rejection. The Office's attention is respectfully directed to page 8, line 30 to page 9, line 3 of the above-identified patent application which states, "In order for each amplifier to truly represent the pixel value onto the common video bus, the amplifier must charge or discharge the bus with in one pixel time constant. It must be stable long enough for a sample and hold circuit (or similar) to accurately present the resultant signal to an A to D converter. A conservative engineer will want at least 5τ (tau or time constants) to accurately allow the video bus to settle to the video value presented by each individual column amplifier." As discussed at page 10, lines 1-3 of the above-identified patent application, "The high speed, low noise, low power analog PVS bus for imagers as shown in FIG. 7 utilizes either a standard sequential or random access decoders for selection of a particular column." As discussed at page 10, lines 15-18 of the above-identified patent application, "The purpose of selecting the current column and pre-selecting the next three columns is to allow the video bus to charge up to the proper value and settle prior to being multiplexed by circuit 24 as shown in Figure 7." Accordingly, in one example by simply controlling the opening and closing of the switches shown in FIG. 7 in the manner described above, the control system is able to substantially charge one of the signal buses which is not being currently read at the output. In view of the foregoing remarks, the Office is respectfully requested to reconsider and withdraw the rejection of claims 32-48.

In view of the above, reconsideration of the outstanding Office action is respectfully requested. Pursuant to 37 CFR § 1.121, attached as Appendix A is a Version With Markings to Show Changes Made.

In view of all of the foregoing, Applicant submits that this case is in condition for allowance, and such allowance is earnestly solicited.

Respectfully submitted,

Date: Sept. 27, 2002

Gunnar G. Leinberg
Registration No. 35,584

NIXON PEABODY LLP
Clinton Square, P.O. Box 31051
Rochester, New York 14603
Telephone: (585) 263-1014
Facsimile: (585) 263-1600

B

OIPE JC87 SEP 30 2002 PATENT & TRADEMARK OFFICE

RECEIVED OCT -7 2002 TECHNOLOGY CENTER 2800

Appendix A

Version With Markings to Show Changes Made

In reference to the amendments made herein to the specification, additions appear as underlined text, while deletions appear as bracketed text, as indicated below:

In The Specification:

Please amend the specification as follows:

The paragraph beginning at page 5, line 1 has been amended as follows:

The active pixel 50 of the prior art includes a photogate 60 and a transfer gate 62 that are used to couple photo generated charge onto the floating diffusion node 52 which is connected to the gate 56 of source follower 53. The drain of the output FET 53 is connected directly to a power supply rail VDD. The source follower output FET is in turn connected to the source [56] 57 of row access FET 58. When the row access FET 58 is selected for reading, the FET 58 is turned on, allowing output FET 53 to be connected to a load 18 and drive the CDS circuitry 55 directly.

The paragraph beginning at page 5, line 30 has been amended as follows:

The [source] drain 30 of FET 24 is the output of the differential pair and is connected to CDS 34.

The paragraph beginning at page 10, line 15 has been amended as follows:

The purpose of selecting the current column and pre-selecting the next three columns is to allow the video bus to charge up to the proper value and settle prior to being demultplexed by [as shown in Figure 7] circuit 24 as shown in Figure 7. By pre-selecting the three columns (or pixel time constants) ahead of time, the column video processing circuitry only has to drive the video bus at one quarter the actual pixel read rate (one-fourth the bandwidth) and therefore can be made smaller and lower power than they would otherwise have to be. Also, since each column is connected to only one out of every four columns the video bus has only one-fourth of the capacitance, because there are only one fourth of the transmission gates (or switches) to drive. As a result, each column selected also pre-selects

the next three columns in sequence. The column selection sequence remains conventional, with out the need for post processing reconstruction of the original image required of multi-port imagers. The analog pre-charging is done at a one-fourth the bandwidth in Figure 7 than the prior art conventional single ended video bus and only the demultiplexing is done at the normal bandwidth.